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Abstract

In this paper, we design a folded cascode operational transconductance amplifier in a standard CMOS process, which has a measured $69\,\mathrm{dB}$ *DC gain, a* $2\,\mathrm{MHz}$ *bandwidth and compatible input- and output voltage levels at a* $1\,\mathrm{V}$ *power supply. This is done by a novel Current Driven Bulk (CDB) technique, which reduces the MOST threshold voltage by forcing a constant current though the transistor bulk terminal. We also look at limitations and improvements of this CDB technique.*

1. Introduction

One of the most serious design constraints when making integrated analogue circuits for systems with low supply voltages is the value of the MOS threshold voltage V_{th}. Several approaches to ultra low voltage supply circuit design have recently been described; eg. based on charge pumps [1], bulk drive [2] or floating gates [3]. In this paper we shall design a standard topology folded cascode Operational Transconductance Amplifier (OTA) which work on a $1\,\mathrm{V}$ power supply by using a technique to lower the MOST threshold voltage.

2. Current driven bulk

The threshold voltage of a MOS transistor as a function of the bulk-source voltage V_{BS} is given by

$$V_{\mathrm{th}} = V_{\mathrm{th0}} + \gamma \left(\sqrt{|2\phi_{\mathrm{F}} - V_{\mathrm{BS}}|} - \sqrt{|2\phi_{\mathrm{F}}|} \right) ,$$

where V_{th0} is the zero bias threshold voltage, γ is the bulk effect factor, ϕ_{F} is the Fermi potential. For p-channel transistors, $2\phi_{\mathrm{F}} \approx -0.7\,\mathrm{V}$ and $\gamma \approx -0.5\,\sqrt{\mathrm{V}}$, typically. By biasing $V_{\mathrm{BS}} < 0\,\mathrm{V}$ we can (numerically) *decrease* the threshold voltage [4, 5].

To reduce the threshold voltage as much as possible, we want the bulk bias $|V_{\mathrm{BS}}|$ as high as possible. This will, however, forward bias the base-emitter diode of the associated parasitic bipolar transistor (BJT) [6]. Now, this is the idea of the new *current driven bulk* (CDB) circuits, see figure 1: we force a current, $I_{\mathrm{BB}} = I_{\max}/(\beta_{\mathrm{CS}}+\beta_{\mathrm{CD}}+1)$, through the diode, where the β's are the two base-collector current gains of the BJT and $I_{\max}$ is the largest emitter current we will allow. Simulations on the threshold voltage as a function of the bulk bias current can be found in [7]. To keep the BJT current gains as low as possible, the layout shown in figure 1C can be used: to keep the substrate-collector gain (β_{CS}) low, the bulk connection is completely surrounded by the source junction; to keep the drain-collector gain (β_{CD}) low, a longer than minimum MOS channel length should be used.

3. CDB unwanted effects

Current driving the bulk introduces a number of unwanted effects in the resulting device. One is the parallel connection of the BJT emitter/collector with the MOS source/drain; this lower the device output impedance. If the BJT emitter current is much smaller than the MOS source current, the effect is negligible. If not, to get a reasonable output impedance, the BJT must be in the active region.

The largest current available for discharging the bulk-drain capacitance is I_{BB}; likewise, the largest current available for charging it is the source quiescent current divided by the base emitter current gain: $I_{\mathrm{S}}/(\beta_{\mathrm{CS}} + \beta_{\mathrm{CD}} + 1)$. This might cause slew-rate effects if the bulk-drain voltage is changed. Together with the bulk transconductance and the base-emitter impedance, the drain-bulk capacitance also causes a low frequency pole-zero pair [7].

As both the slew-rate and the pole-zero pair are caused by the drain-bulk current due to a non-constant bulk-source voltage, both effects can be cancelled by placing a decoupling capacitor between bulk and source. If the source is at a constant potential, a cascode can be used to keep the drain potential constant, thus eliminating the current in the capacitor.

4. Ultra low voltage amplifier

Figure 2 shows our OTA. It is a standard folded cascode transconductance amplifier with a CDB differential pair, and a CDB output current mirror (for simplicity a straight-

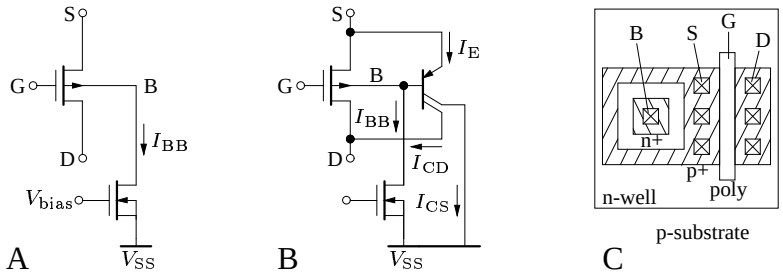

Figure 1. Current drive of bulk terminal. A) circuit B) with parasitic BJT C) layout.

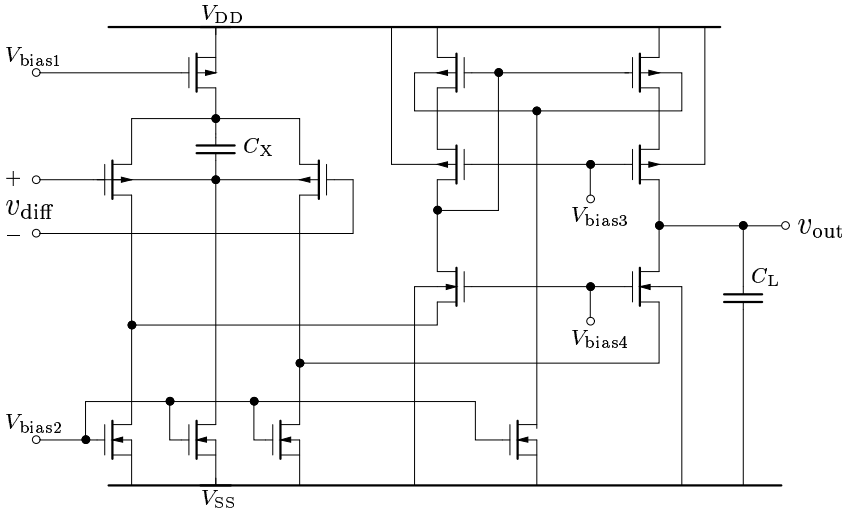

Figure 2. 1V CDB folded cascode OTA.

forward bias circuit is shown). Assuming a standard, strong inversion design with $V_{DD} = 1\,V$, $V_{SS} = 0\,V$, $|V_{th}| = 0.6\,V$ and $V_{DS,sat} = 0.1\,V$, the range of the input common-mode voltage would be $-0.5\,V \lesssim V_{CM} \lesssim 0.2\,V$, which is not compatible with the output voltage range $0.2\,V \lesssim v_{out} \lesssim 0.8\,V$.

Reducing the threshold voltage of the differential pair directly improves the common-mode input range. Also, operating the input pair in sub-threshold reduces the gate-source voltage, and improves the common-mode input range. Assuming we can reduce the threshold voltage till $|V'_{th}| = 0.4\,V$ by current driving the bulk, we now get $-0.1\,V \lesssim V'_{CM} \lesssim 0.6\,V$, and have a $0.4\,V$ overlap in the valid in- and output ranges. To get more voltage room for the current mirror, we also current drive the bulk of the transistors in this.

As the drains of all the current driven bulk transistors are cascoded, we will not expect any parasitic poles from the CDB technique. However, when a large common-mode input signal change is applied, the bulk-drain voltage of the input pair will change, which might cause slewing in this stage. We reduce this slewing effect by adding a coupling capacitor C_X between the bulk and the source of the pair.

An experimental amplifier has been fabricated in a standard $0.5\,\mu m$ CMOS process. It has been designed with a quite high total bias current, $40\,\mu A$, such that it can drive a $20\,pF$ off-chip capacitive load while having a $1\,MHz$-range gain-bandwidth (a version for on-chip applications is straight-forward to do by transistor scaling). The coupling capacitor C_X can be chosen to $10\,pF$ or $0\,pF$. The nominal value of the bulk current is $I_{BB} = 10\,nA$, which (given a BJT current gain of about 100) gives a $10\,\%$ increase in differential pair quiescent current. The strong inversion transistors have been designed to operate with a $100\,mV$ effective gate-source voltage.

Figure 3 shows the measured DC transfer function of our amplifier for different common-mode input voltages, using a $1\,V$ power supply. Figure 4 shows the DC transfer function using a $0.75\,V$ power supply; this figure also show the transfer function when no transistors are driven with a bulk current. It is evident that our CDB technique enables us to use this ultra low power supply. Figure 5 shows the DC gain as a function of the common-mode input voltage. We see, that at a $1\,V$ power supply, we have a $0.65\,V$ common-mode input range in which the amplifier has at least a $62\,dB$ gain; and an overlap of about $0.3\,V$ in the input- and output voltage ranges. Figure 6 compares the measured and simulated AC characteristics of the amplifier when loaded with $20\,pF$. Apart from a slightly worse phase margin, measurements and simulations agree very well. Quantitatively, the measurements are the same for all common-mode input voltages; also they are the same regardless of whether C_X is present

Table 1. CDB OTA measured figures of merit.

Supply voltage	1.0 V	0.8 V	0.7 V
Common-mode input range	0.0 V–0.65 V	0.0 V–0.4 V	0.0 V–0.3 V
High gain output range	0.35 V–0.75 V	0.25 V–0.5 V	0.2 V–0.4 V
Output saturation limits	0.1 V–0.9 V	0.15 V–0.65 V	0.1 V–0.6 V
DC gain	62 dB–69 dB	46 dB–53 dB	33 dB–36 dB
Gain-bandwidth	2.0 MHz	0.8 MHz	1.3 MHz
Slew-rate	0.5 V/μs	0.4 V/μs	0.1 V/μs
Phase margin	57 °	54 °	48 °

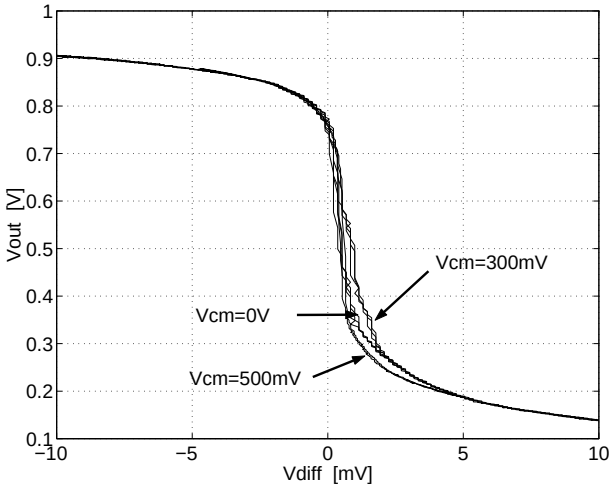

Figure 3. Measured CDB OTA DC responses at $V_{\mathrm{DD}} = 1.0\,\mathrm{V}$ at different common-mode voltages.

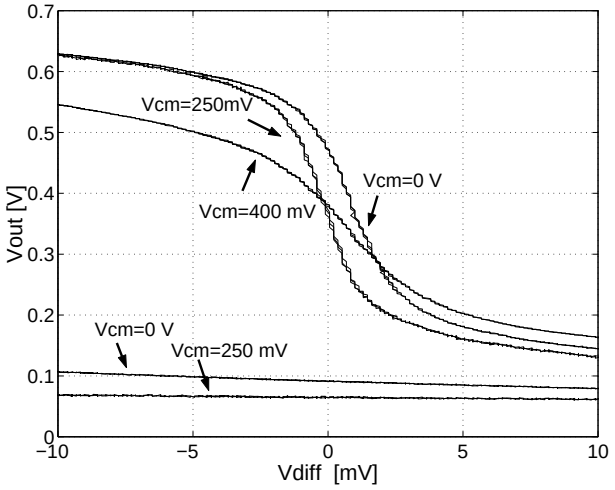

Figure 4. Measured CDB OTA DC responses at $V_{\mathrm{DD}} = 0.75\,\mathrm{V}$ with and without (two bottom traces) bulk current.

or not. The slew-rate is also virtually independent of the presence of C_{X}, and the CDB induced slewing shows only at a $0.7\,\mathrm{V}$ power supply, which could be because the BJT current gain is low. It has a gain-bandwidth of $2\,\mathrm{MHz}$ and a phase margin of $57\,°$. All respectable data for any $1\,\mathrm{V}$ amplifier.

5. Type II CDB circuit

As we have seen, there are two problems with the basic CDB MOST: the uncertainty of increase in quiescent current because of the unknown BJT current gain, and the trouble associated with the drain-bulk capacitance because of the very small current available to charge this. In [7] we solved the first problem was using a feed-back technique to measure the BJT current gain, and our measurements show that adding cascodes and coupling capacitors can solve the other problem. At the expense of a more complicated circuit, there is another way of solving both problems, though. This, Type II CDB technique, can be seen in figure 7. The idea is to add another collector to the BJT, and then couple the BJT as a current mirror, feeding this a current I_{Q} in replace for the bulk current I_{BB}. Doing this, we will know approximately what the emitter current is (see figure) and hence what the increase in quiescent current is. Also, this technique will give a current I_{Q} for charging the drain-bulk capacitance; i.e. the base-emitter current gain as much current as with the type I CDB circuit. Adding another collector to the BJT requires another MOST if the collectors are to match; also this MOST must be biased as the primary MOST which is most easily done using a current mirror as shown in the figure. This MOST will introduce another parasitic BJT as shown in the figure. Assuming all emitter-collector current gains are approximately the same, this structure will add about $4I_{\mathrm{Q}}$ to the MOST quiescent current. A cross section of the Type II CDB MOST can be seen in figure 8.

6. Conclusions

In this paper, we implemented an ultra low supply voltage folded cascode OTA in a standard CMOS process. At a $1\,\mathrm{V}$ power supply, it has a $0.3\,\mathrm{V}$ overlap in the allowed input common-mode range and the output voltage range, a DC gain of $69\,\mathrm{dB}$ and a $2\,\mathrm{MHz}$ bandwidth. The amplifier works with a power supply of less than $0.8\,\mathrm{V}$ (with a somewhat degraded performance, though). This design was made possible by a new technique to lower the MOST threshold voltage, Current Driven Bulk, where we

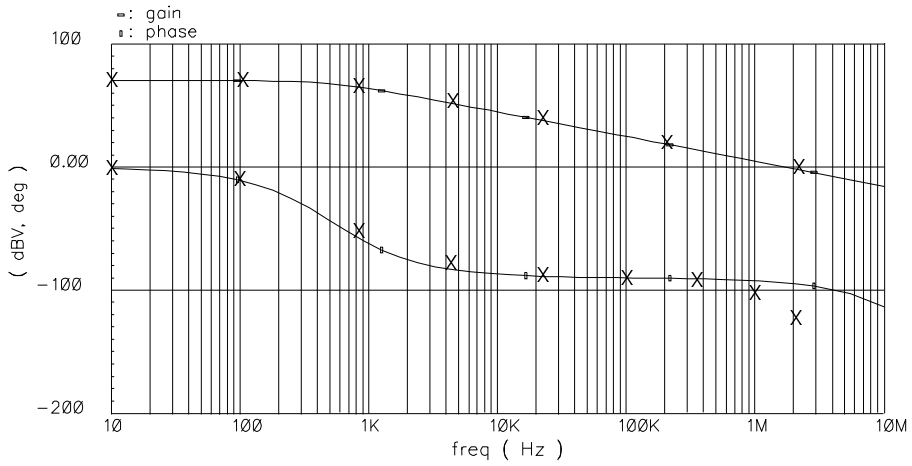

Figure 6. Simulated (—) and measured (X) CDB OTA AC responses.

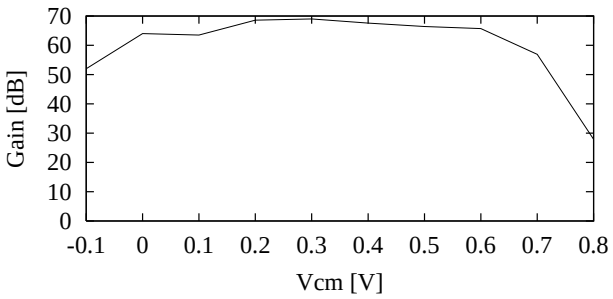

Figure 5. Measured CDB OTA DC gain at $V_{\mathrm{DD}} = 1.0\,\mathrm{V}$.

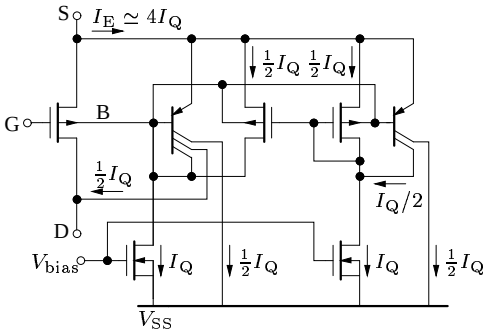

Figure 7. Type II CDB MOST.

force a constant current out of the bulk terminal. Initially, the drain-bulk capacitance gives these circuits poor high-frequency performance, but its effect can be compensated for using cascodes as experimentally verified – or by using additional circuits in the CDB structure.

[1] T. A. F. Duisters and E. C. Dijkmans, "A -90-dB THD rail-to-rail input opamp using a new local charge pump in CMOS," *IEEE J. Solid-St. Circ.*, vol. 33, pp. 947–55, 1998.

[2] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE T. Circuits—II*, vol. 45, no. 7, pp. 769–80, 1998.

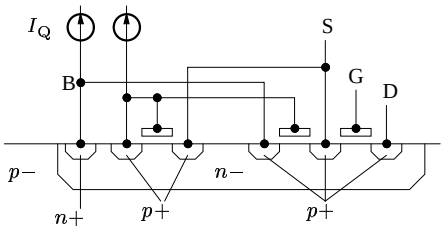

Figure 8. Type II CDB MOST principal physical cross-section.

[3] Y. Berg, D. T. Wisland, and T. S. Lande, "Ultra low-voltage/low-power digital floating-gate circuits," *IEEE Transactions on Circuits and Systems, pt. II*, vol. 46, no. 5, pp. 930–936, 1999.

[4] F. J. D. L. Hidalga-W., M. J. Deen, E. A. Gutierrez-D., and F. Balestra, "Effect of the forward biasing the source-substrate junction in n-metal-oxide-semiconductor transistors for possible low power complementary metal-oxide-semiconductor integrated circuits' applications," *J. Vac. Sci. Technol. B*, vol. 16, no. 4, pp. 1812–17, 1998.

[5] M.-J. Chen, J.-S. Ho, T.-H. Huang, C.-H. Yang, Y.-N. Jou, T. Wu, and T. Wu, "Back-gate forward bias method for low-voltage CMOS digital circuits," *IEEE T. Electron Dev.*, vol. 43, no. 6, pp. 904–10, 1996.

[6] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their application in CMOS technology," *IEEE J. Solid-St. Circ.*, vol. 18, no. 2, pp. 273–279, 1983.

[7] T. Lehmann and M. Cassia, "1V OTA using current driven bulk circuits." Submitted to Journal of Circuits, Systems and Computers, 2000.